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UNITED STATES DISTRICT COURT
NORTHERN DISTRICT OF CALIFORNIA
SAN JOSE DIVISION

VLSI TECHNOLOGY, LLC,

Plaintiff,

v.

INTEL CORPORATION,

Defendant.

Case No. 5:17-cv-05671-BLF-NC

INTEL CORPORATION'S REPLY IN SUPPORT OF ITS OMNIBUS MOTION FOR SUMMARY JUDGMENT

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The exhibits cited in the motion as "Ex. __" are attached to the Declaration of Mark Selwyn filed herewith.

I. INTEL IS ENTITLED TO SUMMARY JUDGMENT OF NO INFRINGEMENT OF THE '836 PATENT.

A. Intel Is Entitled To Summary Judgment Of No Literal Infringement.

The Court should grant summary judgment of no infringement for the '836 patent because (1) the "upon identifying" limitation requires the step of selecting the fastest core to occur ***after*** the step of identifying a single-core task to occur (i.e., selecting after identifying), and (2) Intel's products do the exact opposite by selecting a core ***before*** the determining if only one core is active step that VLSI accuses as identifying a single-core task (i.e., selecting before identifying). Dkt. 579-3 ("Mot.") 2-4. VLSI does not dispute this sequence of steps in Intel's products—which requires summary judgment.

VLSI accuses Intel of "mischaracteriz[ing]" Dr. Conte's opinion about which components are involved in the accused identifying/selecting steps, including the role of p-code. Dkt. 678-2 ("Opp.") 3-4. But Intel did not mischaracterize anything. *E.g.*, Mot. 2-3 (citing Dr. Conte's deposition testimony and expert report describing the role of p-code in the accused selection step). Regardless, Intel's argument turns on the ***order*** that the accused identifying/selecting steps occur, not which components or p-code are involved in those steps. On that issue, because the undisputed evidence shows that Intel's accused products do not select a core after identifying a single-core task as required by the "upon identifying" limitation, summary judgment of no literal infringement should enter.[1]

B. Intel Is Entitled To Summary Judgment Of No Infringement Under The DOE.

Amendment-Based Estoppel: Prosecution history estoppel bars VLSI's DOE theory because

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[1] VLSI points to (1) certain p-code that, [redacted] (which VLSI says is part of selecting a core), and (2) different p-code that, [redacted] (which VLSI says is part of identifying a single-core task). Opp. 2-4. That p-code is involved in both steps says nothing about the order in which they occur, and the fact that the different p-code executes at different times—such that the accused core selection step occurs before the alleged identification of a single-core task—only reaffirms there is no infringement. The Intel documents that VLSI cites, Opp. 2, also do not address the sequence of steps performed by Intel's products, let alone suggest that they select the fastest core upon identifying a single-core task.

the applicants added the "upon identifying" limitation to claim 20 during prosecution for reasons of patentability. Mot. 4-5. VLSI asserts the amendment merely clarified language already in the claim. Opp. 5. But that amendment (1) added an ***entirely new*** temporal limitation to claim 20, and (2) arose from an Examiner interview discussing the obviousness of the claim (over the prior art Bernstein reference), after which the Examiner ***expressly conditioned allowance*** of the claim on making the amendment. That is a classic case of amendment-based prosecution history estoppel. Mot. 4-5.

VLSI posits that the interview could not have related to claim 20 because the Examiner had previously rejected that claim based on Bernstein in combination with Ghiasi, and not the Bernstein/Kim combination discussed during the interview. Opp. 5. But the interview summary identified claim 20 as one of the claims discussed. Dkt. 158-13 ['836 File History] 1934. And the specific amendment to claim 20 that the Examiner required after the interview (to add the "upon identifying" limitation) was consistent with how the applicants distinguished Bernstein during prosecution (on the basis that Bernstein fails to teach identifying single-core tasks). *E.g.*, *id.* 1878-79, 1916 (asserting that because applicants "admitted that 'Bernstein does not specifically teach identifying a processing task that cannot be run by a plurality of cores' … it should be clear that Bernstein does not distinguish between 'multi-core' applications and 'single core' applications").

VLSI contends the amendment bore no more than a tangential relationship to the sequencing of steps required by the "upon identifying" limitation. Opp. 6. But the claim did not require that sequencing before the amendment, and the Examiner's summary explains the language added a temporal sequencing requirement: i.e., "It was ***agreed*** to amend independent claim[] … 20 to clarify that a core is selected from the plurality of cores ***when*** it is identified that a task cannot be run across the plurality of cores." Dkt. 158-13 ['836 File History] 1934 (emphasis added). VLSI also notes claim 20 does not include the word "when," but "upon identifying" imposed the same temporal requirement.

Argument-Based Estoppel: VLSI's DOE theory also is foreclosed because, as the Court found during *Markman*, the applicants made "a clear and unmistakable disavowal" of claim scope during prosecution by representing that the "upon identifying" limitation was missing from the prior art. Mot. 5. VLSI asserts these arguments concerned claim 10, Opp. 6-7, but the *Markman* ruling found that all claims include the same "upon identifying" requirement. Dkt. 241 [*Markman* Order] 22-25. VLSI

also contends the applicants' arguments only concerned whether the prior art disclosed the selecting step, and not the timing of that step. Opp. 7. But VLSI cannot avoid estoppel by trying to separate the requirement to identify a single-core task from the timing for that identification. In any event, the file history is replete with arguments that the claimed invention requires identifying a single-core task before selecting the core on which to run that task. *E.g.*, Dkt. 158-13 ['836 File History] 1876 ("[A] 'single core' processing task is identified. ***Once*** a 'single core' task is identified (a.k.a., a processing task that cannot be run by the plurality of cores), the claimed methodology selects the fastest core to run the 'single core' task." (emphasis added)); *id.* at 1913-14 ("[P]rocessing speed parameters are measured and stored for each of a plurality of cores, and ***upon identifying*** a single-core processing task that cannot be run by the plurality of cores, the core having the fastest measured processing speed parameter is selected to run the identified single-core processing task." (emphasis added)).

Claim Vitiation: VLSI asserts that its DOE theory would not vitiate the "upon identifying" requirement because it permits infringement if the identification/selection steps occur "substantially simultaneously." Opp. 7. But that is precisely the problem. As VLSI and its expert Dr. Conte have conceded, "'upon identifying' … is a temporal term that describes ***when*** something occurs," Dkt. 143 [VLSI *Markman* Br.] 20, and "specifies a predicate" to selecting the fastest core, Dkt. 579-05 [Conte Dep.] 100:9-11. By contrast, VLSI's "substantially simultaneously" theory includes ***any*** ordering of the identification and selection steps—such that the identification step could occur before, at the same time, or after the selection step. Because that would eliminate the temporal ordering provided by "upon identifying," VLSI's DOE theory is foreclosed by the doctrine of claim vitiation.

C. No Infringement Because Intel's Testing Occurs Outside The United States.

VLSI does not dispute Intel performs the testing accused for the "measuring" limitation (claims 1, 9, 20, and 21) ***outside*** the United States—which requires summary judgment of no infringement because method claims are only infringed if all steps are practiced in the United States. Mot. 6-8.

VLSI attempts to avoid the undisputed fact that ***0%*** of the accused testing occurs in the United States by arguing that a stipulation between the parties allows it to treat ***70%*** of that testing as having occurred in the United States. Opp. 8. But nothing in that stipulation purported to allow VLSI to turn indisputably non-infringing activities into infringing activities, or otherwise provides for infringement

by activities occurring outside the United States. To the contrary, the stipulation explicitly states that "[b]y entering into this agreement, ***neither party makes any admission about patent infringement***." Dkt. 581-2 [U.S. Nexus Stip.] 2 (emphasis added). While VLSI asserts that "Intel stipulated that 70% of those activities that meet the technical requirements are deemed to have a U.S. nexus under 35 U.S.C. 271(a)," Opp. 8, VLSI ignores that the "technical requirements" of infringement include the requirement that infringement occur within the United States, *see NTP, Inc. v. Research In Motion, Ltd.*, 418 F.3d 1282, 1318 (Fed. Cir. 2005). The stipulation did not relieve VLSI of its burden to prove infringement of method claims under Section 271(a), which requires not only a U.S. nexus, but also that "***each of the steps***" in that method be "performed ***within this country***." *Id.* (emphasis added).

Only after VLSI meets its burden to show that a product or activity "meet[s] the technical requirements of any asserted VLSI patent claim" can VLSI rely on the stipulation to establish that 70% of Intel's total global sales, revenues, and profits for that product or activity have a U.S. nexus. Dkt. 581-2 [U.S. Nexus Stip.] 2. That is purely an accounting exercise, not an infringement assessment. The stipulation states that this calculation is "without regard to geographic considerations" because the agreed-upon percentage applies to a "total, global number"; the stipulation does not remove geographic considerations from VLSI's proof of infringement (which is a technical predicate to the stipulation applying in the first place). *Id.* And the reference in the stipulation to "each subsection of 35 U.S.C. § 271" is not a shortcut to proving infringement. It simply reflects that the agreed-upon U.S. nexus percentage includes everything covered by § 271 (e.g., making, selling, importing, etc.). Ex. 49 [6/19/18 Letter] (explaining how 70% was calculated).

VLSI's present argument also conflicts with its own conduct in this litigation. For example, over two years ***after*** entering the U.S. Nexus Stipulation, VLSI served a Rule 30(b)(6) notice to Intel that sought testimony on "[t]he place(s) of design, manufacture, assembly, and testing of the Accused Products and their component parts," Ex. 50 [30(b)(6) Notice] 22, and then questioned Intel's corporate designee on the topic for the products accused of infringing the '836 patent, Ex. 51 [Cavagnaro Dep.] 69:19-89:7, 94:11-109:19, 133:8-135:9, 136:6-139:16, 158:7-161:6. If the stipulation meant what VLSI now contends, there would have been no reason to seek that discovery.

Finally, summary judgment also is required for apparatus claims 10-11, 13, and 17, all of which

require "a performance measurement circuit ***for measuring a performance parameter value*** for said core." VLSI does not dispute that the claim language "for measuring" requires the accused products to be "reasonably capable" of performing the claimed function, or that the only place where they have that capability is when attached to an ATE tester at Intel's facilities in Malaysia and Costa Rica. Mot. 7; Opp. 9. VLSI claims that Dr. Conte has established the "technical requirements" necessary to show infringement, but ignores that those opinions are limited to the ATE testing Intel performs overseas. Mot. 7; Dkt. 579-05 [Conte Dep.] 111:4-113:18 (Dr. Conte testifying that he had no opinion and had not considered whether the alleged performance measurement circuit in Intel's products could be used when not connected to an external tester). VLSI also seeks to sidestep its territoriality problem by resorting to the parties' stipulation, Opp. 8, but that argument fails for the same reasons detailed above.

II. INTEL IS ENTITLED TO SUMMARY JUDGMENT OF NO INFRINGEMENT OF THE '922 PATENT.

Intel is entitled to summary judgment of no infringement for the '922 patent because VLSI has failed to identify ***any*** component in the accused products that converts a "reference signal (VSS)," and instead points to the ***same*** VCCIN signal as meeting ***both*** signal requirements (a supply signal VDD ***and*** a reference signal VSS). Mot. 8-9. VLSI's opposition fails to justify a different result.

First, VLSI argues that the claims "do not forbid the claimed 'supply signal' from being the 'reference signal.'" Opp. 9. But the claims do not simply require a generic "supply signal" and a generic "reference signal"; they require a ***specific*** "supply signal (***VDD***)" and a ***specific*** "reference signal (***VSS***)." Dkt. 1-5 ['922 patent], claims 1, 4, 5, 17-18 (emphasis added). That plain claim language "forbid[s]" the same signal from meeting the requirement for both claimed signals because, as even Dr. Mangione-Smith admits, (1) VDD and VSS are known types of signals that have ***different*** voltage levels, and (2) the ***difference*** between VDD and VSS is what defines a circuit's voltage, such that a circuit would have 0 volts (and thus would not work) if VDD and VSS were the same. Mot. 9.

VLSI cites *Powell v. Home Depot U.S.A., Inc*, to argue "[t]here is no legal reason why the same element of an accused product cannot as a general matter satisfy two distinct claim limitations." Opp. 9-10. But Intel is not arguing "as a general matter" that the same structure can never satisfy multiple claim limitations. Rather, as detailed above, Intel's argument turns on the specific wording of the asserted claims, which requires two separate signals. Further, *Powell* merely found that the same

component could satisfy the claim requirements for a "cutting box" and "dust collection structure" where the specification expressly disclosed that the "cutting box may also function as a 'dust collection structure.'" 663 F.3d 1221, 1231-32 (Fed. Cir. 2011). Here, by contrast, the '922 patent ***never*** says that reference signal VSS may also function as supply signal VDD, and instead consistently shows them in ***every embodiment*** as separate signals with separate voltages. Mot. 9 (collecting instances).

Second, VLSI contends that the '922 specification "at most[] only show[s] separate discussion" of VDD and VSS. Opp. 10. That is incorrect. Every embodiment describing VDD and VSS in the same circuit shows them as separate voltages. *E.g.*, Dkt. 1-5 ['922 patent], Figs. 1-7. VLSI's suggestion that the specification does not always label a "reference signal" VSS is incorrect. Opp. 10. In every instance, the specification defines the "reference signal" as "VSS" either explicitly in the text or by referring to a figure that labels the "reference signal" as "VSS." Regardless, the ***claims*** use ***both*** "VDD" and "VSS," and that language controls. VLSI also says the '922 specification states that VDD can have separate or common sources, and multiple components can share VSS. Opp. 10. But the issue here is whether VDD and VSS can share the same signal, and VLSI identifies nothing on this issue—because the '922 patent ***never*** describes VDD and VSS as sharing the same signal. And although VLSI points to Intel's use of "Vcc" or "Vin" in Intel's own documents as shorthand for its input supply voltage VCCIN, Opp. 10, VLSI fails to identify any instance in which Intel used those terms to also refer to a reference signal VSS—again, because VCCIN and VSS are two different things. VLSI also fails to explain how Intel's internal documents could possibly rewrite the scope of the asserted claims.

Third, VLSI argues that Intel and its expert "disregard[] VLSI's opposite expert evidence" about Intel's products. Opp. 10-11. But there is no dispute about how Intel's products work, or that Dr. Mangione-Smith identifies the same VCCIN signal in those products as satisfying both VDD and VSS limitations. The only dispute turns on whether VLSI can satisfy these requirements directed to two different signals with a single signal—an issue of ***claim construction*** that the Court must resolve, and can do so on summary judgment. *See General Mills, Inc. v. Hunt-Wesson, Inc.*, 103 F.3d 978, 983 (Fed. Cir. 1997). VLSI's suggestion that juries can resolve disputes about a claim term's meaning, Opp. 11, violates Federal Circuit law, *see O2 Micro Int'l Ltd. v. Beyond Innovation Tech. Co.*, 521

F.3d 1351, 1360 (Fed. Cir. 2008). VLSI also suggests that a dispute exists as to whether Dr. Mangione-Smith admitted that VDD and VSS are different signals. Opp. 11. But there is no dispute on that issue either, as the deposition record confirms. *Supra* p. 5; Mot. 9; Dkt. 579-11 [Mangione-Smith Dep.] 132:8-24, 137:13-138:3. VLSI cannot avoid summary judgment simply by offering conclusory assertions contradicting Dr. Mangione-Smith's testimony. *See Glaverbel Societe Anonyme v. Northlake Mktg. & Supply, Inc.*, 45 F.3d 1550, 1562 (Fed. Cir. 1995) (requiring "sufficient substance, other than attorney argument, to show that the issue requires trial"); *Disc Golf Ass'n, Inc. v. Champion Discs, Inc.*, 158 F.3d 1002, 1008 (9th Cir. 1998) ("A party cannot create a triable issue of fact, and thus survive summary judgment, merely by contradicting his or her own sworn … testimony[.]").

Finally, VLSI argues that the parenthetical in "reference signal (VSS)" can be ignored as a mere reference to "examples" in the specification. Opp. 11-12. But none of VLSI's cases supports that result. In *NXP USA, Inc. v. Impinj, Inc.*, the court never held that the parenthetical in "specific useful data (nxUDB)" was not limiting; it construed "(nxUDB)" to mean "a number (n) of 'useful data blocks' (UDB)" and limited the claim to "some, but not all, useful data (UD)." 2022 WL 16716226, at *10 (W.D. Wash. Nov. 4, 2022). Here, by contrast, VLSI asks this Court to ascribe "VSS" no meaning at all. Moreover, the parentheticals in *Core Wireless* and *Hochstein* were "reference characters" or "reference numbers" used to identify elements in patent drawings. MPEP 608.01(f); *Core Wireless Licensing S.A.R.L. v. LG Elecs., Inc.*, 2015 WL 6956722, at *5, *7 (E.D. Tex. Nov. 9, 2015) (addressing whether "reference numbers" were limiting); *Hochstein v. Microsoft Corp.*, 2009 WL 1838975, at *12-16 (E.D. Mich. June 22, 2009) (addressing whether "reference characters" were limiting). Here, "VSS" is not a reference character or number. It is a well-known term with an understood meaning in the field, as Dr. Mangione-Smith concedes. Dkt. 579-11 [Mangione-Smith Dep.] 139:3-141:6. Further, the '922 patent distinguishes between reference characters (bolded throughout) and substantive signal names like "VSS" and "VDD" (never bolded). *E.g.*, Dkt. 1-5 ['922 patent], 7:57-8:7, Fig. 4. Thus, just as in *Janssen Pharmaceutica, N.V. v. Eon Labs Manufacturing, Inc.*, the parentheticals here are substantive limitations. 134 F. App'x 425, 428 (Fed. Cir. 2005).

VLSI also argues that "[t]he non-parenthesized 'VSS' in claim 5's 'VSS switch'" supports its position. Opp. 12. But claim 5 uses "VSS switch" to refer back to the term "reference signal (VSS)"

in claim 4—thus confirming that "(VSS)" in claim 4 is limiting and has meaning. Mot. 11. Moreover, VLSI undercuts its position by conceding that "VSS switch" in claim 5 "refers to one of two separately recited switches (the other a 'VDD switch')," and VLSI alleges that it therefore identified "separate" components for the VSS and VDD switches. Opp. 12. That confirms the problem here. The claims also require two "separately recited" signals—a VSS signal and a VDD signal—and it is undisputed that Dr. Mangione-Smith has only identified one signal as meeting both.

III. INTEL IS ENTITLED TO SUMMARY JUDGMENT OF INDEFINITENESS FOR THE '922 PATENT.

VLSI does not explain how the claims could be definite where (1) the patent makes clear that a "power island" is a group of "components with ***similar*** power requirements," but (2) the claims require certain components within the "power island" to have "power characteristics" that are "***different***" (claims 4 and 5) or "***partially different***" (claim 18). Mot. 11-13.

First, VLSI asserts that Intel's indefiniteness argument presents "a highly factual dispute" about "the plain and ordinary meaning of the term ['power island']." Opp. 12, 15. But "indefiniteness is a question of law" that courts can resolve as part of claim construction. *IPXL Holdings, LLC v. Amazon.com, Inc.*, 430 F.3d 1377, 1380 (Fed. Cir. 2005); *ePlus, Inc. v. Lawson Software, Inc.*, 700 F.3d 509, 517 (Fed. Cir. 2012). Indeed, this Court and other courts have found claim terms indefinite before trial. Mot. 12 (citing cases). The only dispute Dr. Mangione-Smith has raised is purely legal—whether "power island" is a limiting term with meaning. *E.g.*, Ex. 52 [Mangione-Smith Reply] ¶ 66.

Second, VLSI argues that "power island" is not limiting because it appears in the preamble of claim 1. Opp. 12-13. But VLSI took the ***opposite*** position during IPRs, in which it admitted that "[c]laim 1 requires the 'conversion controller' to be ***on the power island***," and also relied on claim 1's "power island" requirement to distinguish prior art. Ex. 53 [IPR2018-01033 Sur-reply] 31-32 (emphasis added); *see also* Ex. 54 [IPR2018-01144 Sur-reply] 28-30; Ex. 55 [IPR2018-01033 POR] 66-67.[2] VLSI also ignores that every asserted claim contains one or more ***non***-preamble limitations

[2] Although those arguments concerned unasserted claims 3 and 19, claim 3's "the power island" derives its antecedent basis from claim 1's preamble, and claim 19 depends from claim 4, which depends from claim 1. Dkt. 1-5 ['922 patent], claims 3, 19. The "power island" limitation should be

directed to "***the*** power island." Dkt. 1-5 ['922 patent], claims 4, 17 (emphasis added); *see Eaton Corp. v. Rockwell Int'l Corp.*, 323 F.3d 1332, 1339 (Fed. Cir. 2003) ("When limitations in the body of the claim rely upon and derive antecedent basis from the preamble, then the preamble may act as a necessary component of the claimed invention."). VLSI also dismisses Intel's cited cases "addressing terms of degree" as "inapposite because 'power island' is not a term of degree." Opp. 13. But the patent describes the claimed "power island" as including components with "***similar*** power requirements" that also have "***different***" or "***partially different***" "power characteristics"—i.e., terms of degree. Mot. 11-12; *supra* p. 8. VLSI also asserts that none of these cases "address preamble language," Opp. 13, but that argument also fails because the preamble is limiting (as discussed above).

Third, VLSI argues that Intel waived this indefiniteness issue by not raising it during *Markman*. Opp. 14. But the parties agreed Intel would ***not*** argue during *Markman* that "power island" is indefinite, and expressly noted that "Intel may raise at a later time … such as in an authorized motion for summary judgment[] any indefiniteness arguments as to th[at] term[]." Dkt. 106. VLSI also incorrectly asserts that Intel never disclosed its indefiniteness theory in invalidity contentions or expert reports. Opp. 14. There was no waiver. Ex. 57 [3/19/18 Contentions] 1594-95; Ex. 58 [1/26/22 Contentions] 1377; Dkt. 678-12 [Apsel Rpt.] ¶ 1181; Ex. 59 [Apsel Reply Rpt.] ¶ 666.

Fourth, VLSI argues that first-named inventor Mr. Evoy's testimony—that the meaning of "power island" is "fluid"—does not support Intel when "[v]iewed in context." Opp. 14. VLSI cannot avoid summary judgment based on this conclusory argument. *See TechSearch, LLC v. Intel Corp.*, 286 F.3d 1360, 1371-72 (Fed. Cir. 2002). VLSI also contends that Mr. Evoy's testimony should be disregarded because he did not study the '922 patent or its file history. Opp. 14. But nowhere in the cited testimony did Mr. Evoy ask for those things or qualify his testimony based on his recollection of the patent. Dkt. 585-2 [Evoy Dep.] 96:4-17, 97:23-98:1, 82:22-24. Contrary to VLSI's argument, an inventor's understanding of a claim term is probative. *Markman v. Westview Instruments, Inc.*, 52

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interpreted consistently across these related claims. *See In re Varma*, 816 F.3d 1352, 1363 (Fed. Cir. 2016). VLSI criticizes Intel for not expressly stating in the IPR that the preamble was limiting, Opp. 14-15, but Intel's IPR petitions treated "power island" as limiting, *e.g.*, Ex. 56 [IPR2018-01033] 37.

F.3d 967, 980 (Fed. Cir. 1995) (listing "inventor testimony" as "evidence [that] may be helpful to explain … the meaning of technical terms, and terms of art"), *aff'd*, 517 U.S. 370 (1996).[3]

IV. INTEL IS ENTITLED TO SUMMARY JUDGMENT OF NO INFRINGEMENT OF THE '806 PATENT.

For the '806 patent, VLSI has failed to meet its burden to satisfy the term "when in a second mode of operation," which the Court construed to require that "***both*** the voltage provided to the first memory ***and*** the voltage provided to the second memory must be ***lower than the minimum operating voltage of the first memory***." Mot. 13 (first and second emphases added). This construction has ***two*** requirements: not only must the voltage provided to the ***first*** memory (allegedly the LLC data array) be lower than the first memory's minimum operating voltage, but also the voltage provided to the ***second*** memory (allegedly the DCU state array) must be lower than the first memory's minimum operating voltage. VLSI offered no viable evidence to satisfy these requirements. VLSI concedes its expert Dr. Conte has not identified ***any*** minimum operating voltage for the accused LLC data array. Opp. 15. This admission alone confirms summary judgment is warranted because without any such value, it is impossible to determine whether the voltages provided to either the accused first memory or the accused second memory are lower than the LLC data array's minimum operating voltage.

VLSI contends that "such quantification is not required" because Dr. Conte alleges that "sleep transistors" in Intel's products [redacted]. Opp. 15-16. But it is undisputed that the "sleep transistors" [redacted]. Opp. 16-18. This gap in evidence is fatal to VLSI's claim.

VLSI's opposition states that "when in the second mode of operation, the DCU state array

[3] VLSI notes that in the IPR, Intel's expert cited the specification's statement that a "power island" requires components with "similar power requirements." *See* Opp. 15. But the Board held that even "similar" power requirements are insufficient to decide if components are part of the claimed "power island"—thus amplifying the indefiniteness of this term. Ex. 60 [IPR 2018-01144, FWD] 81-82.

[redacted]." Opp. 17. But it does not explain how that supposedly occurs, and none of its citations do either. Such "conclusory statements are insufficient" to avoid summary judgment. *TechSearch*, 286 F.3d at 1372.

V. INTEL IS ENTITLED TO SUMMARY JUDGMENT OF NO INFRINGEMENT OF THE '672 PATENT.

Intel's current process: Dr. Neikirk admitted that [redacted] is a solid and that the '672 patent does not disclose melting solder ***after*** it has been applied as "provid[ing] solder as a fluid layer." Mot. 17. Moreover, the '672 patent (1) uses "provide" and "apply" interchangeably to describe creating the solder layer, (2) discloses applying only fluid solder as "providing" the solder "of the invention," and (3) distinguishes plated solder for not meeting the patent's goals. Dkt. 1-7 ['672 patent] 1:54-57, 3:23-25, 3:58-61, 4:11-13, 4:18-21, 4:33-35, 4:60-65, 5:12-15, 6:28-43.

VLSI does not dispute any of this. Instead, it asserts that two specification passages support its broad reading of "provide." Opp. 18-19. But the passages simply state that solder, however applied, has "a relatively small height" and that melting solder can achieve "non-planarity tolerance." Dkt. 1-7 ['672 patent] 2:7-8, 2:19-21. Neither passage discusses ***how*** solder is provided "as a fluid layer" or contradicts the remainder of the patent. VLSI also relies on claim 6, but the claim's recitation of immersion soldering ***supports*** that "providing" means "applying": immersion soldering is a method of ***applying*** fluid solder.[4] And none of VLSI's extrinsic evidence suggests that ***transforming*** solder from a solid to a fluid ***after*** it is applied is "providing" solder. In fact, VLSI's evidence demonstrates that solder cannot be "provided" ("made available" or "supplied") if it is already present, as VLSI's infringement theory requires. Opp. 19. At bottom, ***none*** of the evidence suggests that melting and/or transferring already applied solder in a later process satisfies the "providing" as a fluid layer step.

Intel's discontinued process: VLSI fails to identify any evidence that Intel's old [redacted] process meets the contact angle limitation. VLSI quotes a portion of a single Intel document that it

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[4] Limiting claim 1 to immersion soldering (which Intel has not argued) would not violate claim differentiation (as VLSI suggests) because claim 6 contains other limitations not present in claim 1 and there are other methods of applying fluid solder covered by claim 1. Ex. 61 [Fay Dep.] 182:19-183:6; *see Andersen Corp. v. Fiber Composites, LLC*, 474 F.3d 1361, 1370 (Fed. Cir. 2007).

contends "[redacted]." Opp. 19-20. But VLSI did not even submit the document as an exhibit, much less explain it. And Dr. Neikirk's opinions provide no assistance: his reports never discuss the document. Dkt. 678-19 [Neikirk Reply] ¶ 61; Dkt. 678-18 [Neikirk Rpt.] ¶¶ 252-55; Opp. 20. In any event, the document contains no such admission: [redacted]. Ex. 62 [redacted] 1, 6, 7; Ex. 67 [Jen Dep.] 5:18-21, 65:24-68:16. Critically, [redacted], which is ***not*** the claimed contact angle between the solder and the ***horizontal*** underbump metallization. Ex. 62 [redacted] 4. VLSI does not explain how this document—or any other alleged evidence—demonstrates that Intel performs the claimed steps. Mot. 19-20.

VLSI instead resorts to an alleged "scientific principle," Opp. 20, which is contradicted by VLSI's asserted support and untethered to evidence of Intel's ***actual*** processes, Mot. 18. Although VLSI suggests that providing images of [redacted] contact angle would be impossible, that is not so: Intel produced evidence of [redacted], including images. Intel engineers testified that Intel [redacted], and Intel produced documents showing the results. Ex. 63 [Baldwin Dep.] 37:6-38:6; Ex. 64 [redacted] 10; Ex. 65 [redacted] 2. Intel's expert discussed this process and demonstrated that [redacted]. Ex. 66 [Fay Reb.] ¶¶ 73, 158-59; Ex. 67 [Jen Dep.] 64:10-17. Dr. Neikirk never addressed or rebutted this evidence. Dkt. 678-19 [Neikirk Reply] ¶¶ 59-62.

Finally, VLSI asserts that Dr. Neikirk visually inspected a single, unidentified image and "concluded that [redacted]°." Dkt. 678-18 [Neikirk Rpt.] ¶ 256. But that cannot raise a genuine issue of fact. Dr. Neikirk failed to identify the location of any contact angle in the cited image, let alone measure or calculate a [redacted]°. Furthermore, as VLSI admits, the image shows [redacted], which is not relevant to the claimed contact angle, which must be made when the solder is provided as a fluid layer.

VI. INTEL IS ENTITLED TO SUMMARY JUDGMENT ON ITS LICENSE DEFENSE.

As explained in both Intel's motion, Mot. 18-21, and Intel's opposition to VLSI's motion, Dkt.

671-3 at 1-11, Intel is licensed to practice VLSI's patents. VLSI's arguments otherwise lack merit.

First, VLSI argues that Fortress, Finjan, and VLSI do not "own" each other, that "VLSI and Finjan have nothing to do with each other," and that VLSI was created after execution of the License. Opp. 21-22. But VLSI is an "Affiliate" because (1) the License defines "Affiliates" as those under "common control" of the "Finjan Parties," including future entities and without requiring common ownership, and (2) Fortress exercises common control over VLSI and Finjan [redacted]. Mot. 19; Dkt. 671-3 at 2-4. VLSI's cited cases, Opp. 21; *see also* Dkt. 588-2 at 15, focus on different issues of control than are at issue here and do not involve situations in which an entity [redacted] of multiple patent assertion entities.

Contrary to VLSI's blanket assertions, Opp. 22, non-signatories to an agreement (or later-created entities) can be bound where the non-signatory meets the agreement's definition of "Affiliate." Mot. 20 (collecting cases); *Acquisitions and IP Licenses: Looking Out for Poison Pill Affiliate*, 249 N.Y. L.J. 2 (2013). VLSI incorrectly claims that Intel's cited cases apply only to "'affiliates' created by and 'under the control of a party to the agreement.'" Opp. 22. In *Shorenstein*, for example, the direct party to the agreement was CSH, but the Delaware Supreme Court held the agreement bound CSH's owner (the Hays) and a separate theater Carole Hays owned. 213 A.3d 39, 42, 56-57 (Del. 2019); *see id*. 42 n.2, 43 n.4. That is directly analogous to the License here binding Fortress and VLSI.

Second, VLSI asserts that its patents are not "Finjan's Patents" because "NXP and others hav[e] ongoing financial interests in royalties." Opp. 22. But VLSI is not [redacted], and VLSI has identified no evidence that [redacted]. Dkt. 671-3 at 5-6.

Finally, VLSI argues that Intel's defense is precluded. Opp. 21. But claim preclusion does not apply because the causes of action in the Texas action and this case involve different patents, different accused products, and different features from the patents and accused products. Dkt. 671-3 at 11-13 (collecting cases). Likewise, issue preclusion does not apply because the Texas order denying Intel leave to amend did not resolve the issue of common control and rested primarily on an alleged procedural default, so—contrary to VLSI's assertion—the court's additional finding that Intel's defense was futile was not essential to the judgment. Mot. 20-21; Dkt. 671-3 at 13-15.

VII. INTEL IS ENTITLED TO SUMMARY JUDGMENT OF NO WILLFUL OR INDIRECT INFRINGEMENT, AND NO ENHANCED DAMAGES.

Summary judgment of no willful or indirect infringement should enter because the undisputed record shows that Intel lacked the requisite knowledge of both the asserted patents and its alleged infringement, and summary judgment of no enhanced damages should enter because VLSI has not offered evidence sufficient to prove that Intel committed the type of "egregious" conduct required for enhanced damages. Mot. 21-24. VLSI's opposition confirms that summary judgment is warranted.

No Willful or Indirect Infringement: In its brief, VLSI does not identify any evidence that anyone at Intel knew about both (1) the asserted patents and (2) any Intel infringement of those patents. VLSI instead attempts to impute such knowledge to Intel, but none of its arguments has merit.

First, VLSI alleges that "Intel regularly monitors competitors' (including NXP's) activities, and has acknowledged its competitors have patents covering similar products." Opp. 23. That argument is (1) waived because VLSI did not raise it in its complaint or contentions, and (2) irrelevant and misleading given that VLSI admits that [redacted]. Ex. 68 [VLSI Interrog. Resp.] 6. Nor did VLSI's cited cases find the requisite knowledge based on mere monitoring of competitors' activities. *See WCM Indus., Inc. v. IPS Corp.*, 721 F. App'x 959, 971 (Fed. Cir. 2018); *Dentsply Sirona, Inc. v. Edge Endo, LLC*, 2019 WL 1517584, at *4 (D.N.M. Apr. 8, 2019).

Second, VLSI notes that Intel "cited the ['836] patent's application during prosecution." Opp. 23. But at most, that shows pre-suit knowledge of that patent, and is irrelevant to VLSI's burden to prove that Intel knew it infringed that patent (or the other asserted patents). Indeed, consistent with Intel's cited cases, Mot. 22, VLSI's sole cited case found that "citing a patent application" during prosecution was ***insufficient*** to establish pre-suit knowledge of infringement. *MasterObjects, Inc. v. Amazon.com, Inc.*, 2021 WL 4685306, at *4 (N.D. Cal. Oct. 7, 2021).

Third, VLSI asserts willful blindness based on claims that "Intel has a policy discouraging engineers from looking at third-party patents." Opp. 23-24. Because VLSI also never raised this argument in its contentions, it is waived. Further, the assertion cannot avoid summary judgment given that Intel's engineers merely explained their practice not to look at others' patents (to avoid being

"influenced"), and instead focused on their own "innovations." Dkt. 678-21 [Chen] 12:10-13:11; Dkt. 678-10 [Therien] 394:20-396:21. VLSI cites no case where such testimony was found to amount to willful blindness and no evidence linking its allegations about Intel's supposed "policy" to the asserted patents. VLSI also alleges no facts remotely close to those in *Global-Tech Appliances, Inc. v. SEB S.A.*, which found willful blindness because the accused infringer intentionally copied its competitor's product, despite knowing patents likely covered the copied design. 563 U.S. 754, 770-71 (2011).

Fourth, VLSI argues that Intel had sufficient post-suit knowledge based on the filing of the complaint. Opp. 24. But multiple courts—including in this District—have rejected reliance on a complaint to establish the knowledge needed for willful and indirect infringement. Mot. 22 (collecting cases). Consistent with those decisions, the Federal Circuit has affirmed the dismissal of indirect infringement claims for lack of sufficient knowledge, even after the filing of a complaint. *See, e.g.*, *Artrip v. Ball Corp.*, 735 F. App'x 708, 713 (Fed. Cir. 2018); *Addiction & Detoxification Institute LLC v. Carpenter*, 620 F. App'x 934, 938 (Fed. Cir. 2015). Moreover, even if VLSI relies on its complaint for post-suit knowledge of the patents, it has failed to identify evidence showing ***knowledge of infringement***—because every Intel witness questioned on the subject testified that Intel does not infringe and VLSI alleges "no more than ordinary infringement" since filing the case. Mot. 23-24.

Finally, VLSI points to other U.S. litigation with Intel, Opp. 25, but ignores that (1) it has lost on or dropped 14 of its 21 patents asserted against Intel, (2) for each of the 3 patents Intel was found to infringe, VLSI lost or dropped its willful infringement claims, and (3) for those 3 patents, the Patent Office has since found 2 of the patents invalid (and the infringement judgment for those patents is still on appeal), and the other patent is still the subject of post-trial motions. Thus, if anything, the litigation history between the parties only reinforces Intel's subjective belief that it does not infringe.

No Enhanced Damages: VLSI argues that the "normal practice" requires deferring a decision on whether it can prove enhanced damages until after "the jury finds Intel willfully infringed." Opp. 25. But as detailed above, the jury should not be allowed even to consider VLSI's willful infringement claims. Summary judgment of no enhanced damages also is warranted because VLSI does not identify any facts sufficient to show "'egregious' conduct that would warrant enhanced damages under *Halo*." *See Finjan, Inc. v. Cisco Sys. Inc.*, 2017 WL 2462423, at *5 (N.D. Cal. June 7, 2017) (Freeman, J.).

Respectfully submitted,

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